Interview questions for Fermionic design (AMS verification)

1. Started with the brief introduction.
2. Based on specifiations how you are doing model vs schematic for LDO
3. What is config and why we are using it..
4. How you are applying to stimulus model and Schematic (AMScf file)
5. What are tools used for only schematic and Verilog-a model simulation
6. Explain the operation PLL from the block-digram..asked we you are arbitrary frequency divider(%N).
7. Difference between Verilog-ams and wreal modelling
8. Modelling pfd in PLL using Verilog-a/sv/wreal…(complete behavioural level only without using dff and nand gate which becomes a structural modelling)
9. Explain the design the 5-OTA
10. RC low pass and high pass filter with pulse input with different time periods.
11. What is make file and SV testbench architeure, protocols(spi, i2c) and which protocol is faster. Do you python